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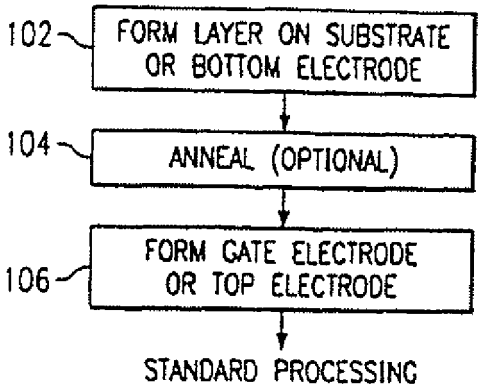
(54) Chemical vapor deposition of silicate high dielectric constant materials

(57) A method of fabricating an electronic device over a semiconductor substrate, the method comprising the steps of: forming a conductive structure over the semiconductor substrate (step 106 of FIGURE 1); and forming a layer of high-dielectric constant material between the conductive structure and the semiconductor substrate (step 102 of FIGURE 1), the layer of high-dielectric constant material is formed by supplying a gaseous silicon source and a second gaseous material which is comprised of a material selected from the group consisting of: Hf, Zr, La, Y, Sc, Ce and any combination thereof.

FIG. 1



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Description

FIELD OF THE INVENTION

[0001] The instant invention pertains to semiconductor device fabrication and processing and more specifically to a method of fabricating a high-dielectric constant material over a semiconductor substrate and to a method of fabricating an electronic device.

BACKGROUND OF THE INVENTION

[0002] The trend in semiconductor device processing is to make the devices smaller so that more devices can be fabricated in a given area. This scale down affects substantially all of the device, so that each feature is scaled down. This is particularly problematic for the gate structure and capacitors, because capacitance is proportional to the dielectric constant of the material situated between the two plates of the capacitor and effective area of the dielectric material. In addition, the capacitance of a structure is inversely proportional to the distance between the two electrodes of the structure. Currently, since SiO_2 is the material of choice for gate dielectrics, the thickness of this layer is decreased to compensate for the scaling down of the area of the capacitor. However, this thinning of the oxide layer is becoming problematic for a couple of reasons. First, as the thickness of the silicon dioxide layer is decreased to below about 3 nm, the leakage through the oxide becomes unacceptably high. In addition, the oxide layer ceases to act as an effective barrier with regards to keeping dopants which are implanted into the gate electrode to increase the conductivity of the gate electrode out of the channel regions. Second, extremely thin layers, unless they are formed from a process which is self-limiting, are very difficult to reproducibly fabricate. Third, any etching away of a thin layer, especially a gate insulator, using subsequent processing to etch other structures affects the thinner layer more dramatically than it would a thicker layer because a greater percentage of the thinner layer is removed than that of a thicker layer.

[0003] Another approach to solve this problem involves changing the gate insulating material to one with a higher dielectric constant. For example, BST, PZT, TiO_2 and Ta_2O_5 are being considered for the next generation of gate dielectrics. However, each of these materials pose problems because the processing required to make these materials into effective gate dielectric materials conflicts with the processing of standard transistor structures. More specifically, each of these materials generally require a high temperature anneal in an oxygen-containing ambient, and this anneal can greatly degrade the underlying substrate and any other exposed oxidizable structures.

[0004] Hence a new material needs to be used which is relatively easy to process using standard gate structure processing techniques and which has a dielectric constant higher than that of silicon dioxide ($\varepsilon \approx 3.9$).

SUMMARY OF THE INVENTION

[0005] Basically, the instant invention involves a gate structure which includes an oxide or a silicate layer as the gate dielectric and a method for fabricating such a structure using chemical vapor deposition (CVD). More specifically, the gate insulator of the instant invention is preferably comprised of $ZrSiO_x$ or $HfSiO_x$ (where $0 < x < 4$), or even ZrO_2 or HfO_2. Preferably, this layer has a dielectric constant of around 10 to 40 (more preferably around 15 to 30). In alternative embodiments, the dielectric layer of the instant invention can be utilized as a capacitor dielectric.

[0006] An embodiment of the instant invention is a method of fabricating a high-dielectric constant material over a semiconductor substrate, the method comprising the steps of: providing a gaseous silicon source in a chamber; providing a second gaseous source in the chamber, the second gaseous source comprised of a material selected from the group consisting of: Hf, Zr, La, Y, Sc, Ce and any combination thereof. The method of the instant invention may further comprise the step of: subjecting the high-dielectric constant material to between 600 and 900 C in an ambient. Preferably, the anneal ambient is comprised of: O_2, O_3, N_2, H_2, NH_3, and any combination thereof. The gaseous silicon source is, preferably, comprised of: silane, disilane, dichlorosilane, and any combination thereof, and may include a carrier gas (preferably comprised of: He, N_2, Ar, and Ne). Preferably, the material is comprised of: $Zr(OC_4H_9)_4$, $Hf(OC_4H_9)_4$, $Zr(NO_3)_4$, $Hf(NO_3)_4$, $ZrCl_4$, $HfCl_4$, ZnI_4, HfI_4, $ZrBr_4$, $HfBr_4$, $Zr_2(OPri)_6(tmhd)_2$, $Hf_2(OPri)_6(tmhd)_2$, and any combination thereof. The second gaseous source may include a source of oxygen.

[0007] A method of fabricating an electronic device over a semiconductor substrate by use of the beforementioned method comprises the further steps of: forming a conductive structure over the semiconductor substrate; and forming the layer of high-dielectric constant material between the conductive structure and the semiconductor substrate. The method of instant invention may also include the step of: subjecting the electronic device to between 600 and 900 C in an ambient. Preferably, the electronic device may be a capacitor or a transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008]

FIGURE 1 is a flow diagram illustrating the method of one embodiment of the instant invention.

FIGUREs 2a-2c are cross-sectional views of a par-

tially fabricated device which is processed using the method of the instant invention as is illustrated in FIGURE 1.

[0009] Like reference numerals in the different figures represent like or similar features. Features illustrated in the figures are not necessarily to scale.

DETAILED DESCRIPTION OF THE DRAWINGS

[0010] While the following description of the instant invention is centered around the methodology of FIGURE 1 and the device structure of FIGUREs 2a-2d, the instant invention can be used with a metal gate or any other type of gate structure and it can be fabricated using a disposable gate or using the standard process flow as is shown. The dielectric layer of the instant invention may also be used as the gate dielectric in a disposable gate structure process flow as is illustrated in co-pending U.S. Patent Application _____ (assigned to TI and docketed as TI-24776P), which is herein incorporated by reference. In addition, the methodology of the instant invention and the dielectric layer formed, thereby, can be used as the dielectric between two electrodes of a capacitor.

[0011] Prior processing may be performed prior to the method of the instant invention. This prior processing may include cleaning the surface of the wafer 202, formation of isolation areas 204, and doping of portions of the wafer. Isolation structures 204 are illustrated in FIGUREs 2a-c as shallow trench isolation structures (STI) but any type of isolation structure may be used. Examples of isolation structures include, LOCOS, STI, and junction isolation structures.

[0012] In most standard processing regimes a thin oxide is grown on the wafer prior to the formation of the isolation structure and implanting of the substrate dopants. If a thin oxide layer is used it would, preferably, be removed prior to step 102. Preferably, the removal of the thin oxide layer is accomplished in an oxide etch, or deglaze, step. This process will, preferably, include subjecting the wafer to an HF solution so as to remove the protective oxide while not substantially affecting isolation structure 204.

[0013] Referring to step 102 of FIGURE 1 and FIGURE 2a, a layer 206 is blanketly formed over substrate 202. In step 102, layer 206 may not be formed on isolation structure (shown in FIGURE 2a), preferably by a masking operation, it may be selectively removed from isolation structure 204, or it may be formed on isolation structure 204 (not shown) and left there. Preferably, layer 206 will be comprised of a transition metal (such as Hf, Zr, La, Y, Sc, and/or Ce), silicon (if layer 208 is to be a silicate) and potentially oxygen and/or nitrogen. Preferably layer 206 will be comprised of $HfSiO_x$, $ZrSiO_x$, $LaSiO_x$, $YSiO_x$, $ScSiO_x$, $CeSiO_x$, Hf, $HfSi_2$, Zr, $ZrSi_2$, La, $LaSi_x$, Y, YSi_x, Sc, $ScSi_x$, Ce, or $CeSi_x$, and is preferably on the order of 4 to 10 nm thick (more preferably around 4 to 6 nm thick). Using the method of the instant invention, layer 206 is formed using chemical vapor deposition. Several embodiments of the instant invention can be used to form the silicate layer of the instant invention.

[0014] In each of the following embodiments, the symbol M is used to designate Hf or Zr or other such metal which have the desired properties similar to Hf and Zr for this application (such as La, Y, Sc or Ce listed above). Each of these embodiments utilize a precursor which is either combined with a carrier gas (which may be comprised of He, nitrogen, argon, neon, or any combination of the above) or not. Preferably, the precursors of the embodiments of the instant invention are comprised with a metal source, M, a silicon source (preferably silane, disilane, and/or dichlorosilane), and possibly even a source of oxygen and/or nitrogen. The source of oxygen can be O_2, O_3 or other oxygen source, such as a plasma source. If a source of oxygen and/or nitrogen is not provided in the precursor, anneal step 104 can be performed so as to incorporate oxygen and/or nitrogen into layer 206.

[0015] In one embodiment of the instant invention, a combination of $M(NO_3)_4$ in gaseous form is provided into a chamber along with silane, or disilane or dichlorosilane, (along with a carrier gas - preferably around 10% of this gas mixture) in gaseous form. Preferably, the flow rate of $M(NO_3)_4$ is around 5 to 20 sccm (more preferably around 10 sccm) and the flow rate of the silane (and carrier gas) is around 1 to 20 sccm (more preferably around 1 to 10 sccm). The ambient temperature of the chamber is around 60 to 120°C (more preferably around 70°C) and the substrate temperature is preferably around 200 to 600°C (more preferably around 300 to 500°C). An advantage of this precursor of the instant invention is that it is carbon-free and it is less likely to form excess water.

[0016] In another embodiment of the instant invention, a combination of metal t-butoxide, $M(OC_4H_9)_4$, (preferably along with a carrier gas) in gaseous form is provided into a chamber along with silane (preferably along with a carrier gas - preferably around 10% of the carrier gas and 90% silane) in gaseous form. Preferably, the flow rate of $M(OC_4H_9)_4$ is around 5 to 15 sccm (more preferably around 10 sccm) and the flow rate of the silane (and carrier gas) is around 1 to 20 sccm (more preferably around 1 to 10 sccm). Disilane or dichlorosilane can be used in place of the silane. The ambient temperature of the chamber is preferably around 60 to 120°C (more preferably around 70°C) and the substrate temperature is preferably around 400 to 700°C (more preferably around 450 to 600°C).

[0017] In another embodiment of the instant invention, the gaseous metal source may be comprised of MCl_4, MI_4, or MBr_4. The gaseous silicon source may be comprised of silane, disilane, or dichlorosilane and may further comprise a carrier gas such as He, Ar, N_2, or Ne. Additionally, a gaseous oxygen source (such as O_2 or

O_3) may be included or a subsequent anneal in an oxygen or ozone ambient may be performed (such as in optional anneal step 104). The substrate temperature during this process is preferably around 200 to 600°C (more preferably around 300 to 500°C). Since chlorine and bromine are very reactive, and since chlorine is corrosive, if either of these gases are used, a non-stainless steel reactor (preferably a quartz reactor) should be used.

[0018] In another embodiment of the instant invention, the gaseous metal source is comprised of $M_2(OPri)_6(tmhd)_2$ and the silicon source is preferably comprised of silane, disilane, or dichlorosilane. Preferably, the substrate temperature during this process is around 400 to 700°C (more preferably around 450 to 600°C). An oxygen source may be used or an anneal in an oxygen or ozone ambient may be performed (such as in step 104).

[0019] Referring to step 104 of FIGURE 1 and FIGURE 2b, an anneal is performed next, if at all, so as to improve the electrical properties of layer 206, which contains a combination of silicon and the transition metal, or more preferably to improve the quality of already existing silicate layer. For example, if layer 206 is comprised of Hf, $HfSi_2$, Zr, or $ZrSi_2$ it would become HfO_x, $HfSiO_x$, ZrO_x, or $ZrSiO_x$, respectively, or more preferably if the layer is already $HfSiO_x$, an anneal step in forming gas (preferably using 90% N_2:10% H_2) will remove the defects in the silicate film, thereby improving the electrical properties of the layer. Alternatively, an anneal in an oxygen-containing ambient will increase the oxygen content of the silicate by increasing the x value. Preferably, anneal step 104 is either performed: in an 90% N_2:10% H_2 ambient at a temperature around 350 to 500°C (more preferably around 450°C) for around 10 to 30 minutes (more preferably 30 minutes); in an O_2 ambient at a temperature around 400 to 900°C (more preferably around 800°C) for around 15 to 60 seconds (preferably around 30 seconds); in an O_3 ambient at a temperature around 25 to 400°C; or in an N_2 or NH_3 ambient at a temperature around 500 to 600°C. Other temperature and ambient combinations may be used but these seem to give the best results. Preferably, layer 206 is subjected to this elevated temperature in an oxygen-containing and/or nitrogen-containing atmosphere for a period of between 10 and 120 seconds (more preferably around 20 to 45 seconds - even more preferably around 30 seconds) in anneal step 104.

[0020] Referring to step 106 of FIGURE 1 and to FIGURE 2c, a conductive gate electrode layer 210 is formed. Preferably, layer 210 is comprised of polycrystalline silicon, polycrystalline silicon germanium, doped polycrystalline silicon, doped polycrystalline silicon germanium, tungsten, titanium, tungsten nitride, titanium nitride, platinum, aluminum, a combination thereof or a stack comprised of one or more of the above. Layer 210 is preferably formed using standard semiconductor processing steps and is of a thickness which is commonly used in standard transistor formation.

[0021] Although specific embodiments of the present invention are herein described, they are not to be construed as limiting the scope of the invention. Many embodiments of the present invention will become apparent to those skilled in the art in light of methodology of the specification. The scope of the invention is limited only by the claims appended.

Claims

1. A method of fabricating a high-dielectric constant material over a semiconductor substrate, said method comprising the steps of:

   providing a gaseous silicon source in a chamber;
   providing a second gaseous source in said chamber, said second gaseous source comprised of a material selected from the group consisting of: Hf, Zr, La, Y, Sc, Ce and any combination thereof.

2. The method of claim 1, further comprising the step of:

   subjecting said high-dielectric constant material to between 600 and 900°C in an ambient.

3. The method of claim 2, wherein said ambient is comprised of a gas selected from the group consisting of: O_2, O_3, N_2, H_2, NH_3, and any combination thereof.

4. The method of claim 1, wherein said gaseous silicon source is comprised of a gas selected from the group consisting of: silane, disilane, dichlorosilane, and any combination thereof.

5. The method of claim 4, wherein said gaseous silicon source includes a carrier gas.

6. The method of claim 5, wherein said carrier gas is comprised of a gas selected from the group consisting of: He, N_2, Ar, and Ne.

7. The method of claim 1, wherein said second gaseous material is comprised of a gas consisting of: $Zr(OC_4H_9)_4$, $Hf(OC_4Hg)_4$, $Zr(NO_3)_4$, $Hf(NO_3)_4$, $ZrCl_4$, $HfCl_4$, ZrI_4, HfI_4, $ZrBr_4$, $HfBr_4$, $Zr_2(OPri)_6(tmhd)_2$, $Hf_2(OPri)_6(tmhd)_2$, and any combination thereof.

8. The method of claim 1, wherein said second gaseous source includes oxygen.

9. A method of fabricating an electronic device over a semiconductor substrate by use of the method of

any of claims 1 to 8, said method comprising the further steps of:

forming a conductive structure over said semiconductor substrate; and
forming the layer of high-dielectric constant material between said conductive structure and said semiconductor substrate.

10. The method of claim 9, further comprising the step of:

subjecting said electronic device to between 600 and 900° C in an ambient.

11. The method of claim 9, wherein said electronic device is a capacitor or a transistor.

FIG. 1

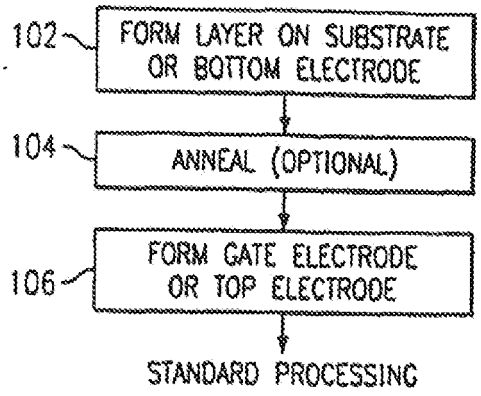

FIG. 2a

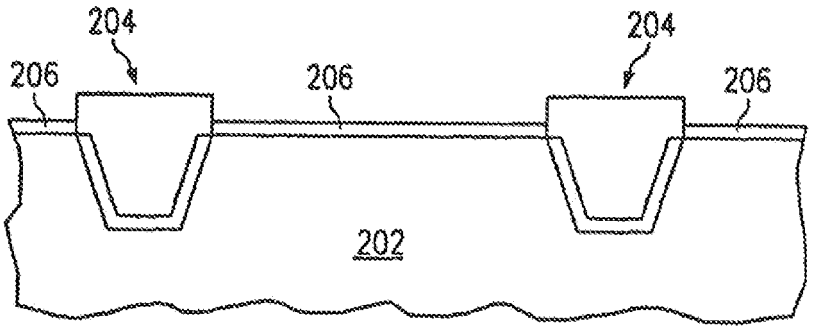

FIG. 2b

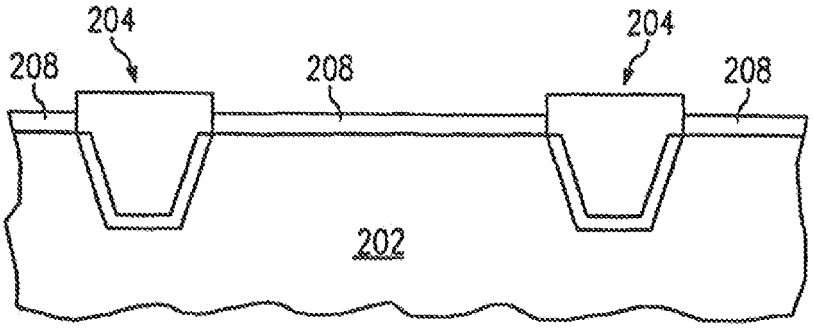

FIG. 2c

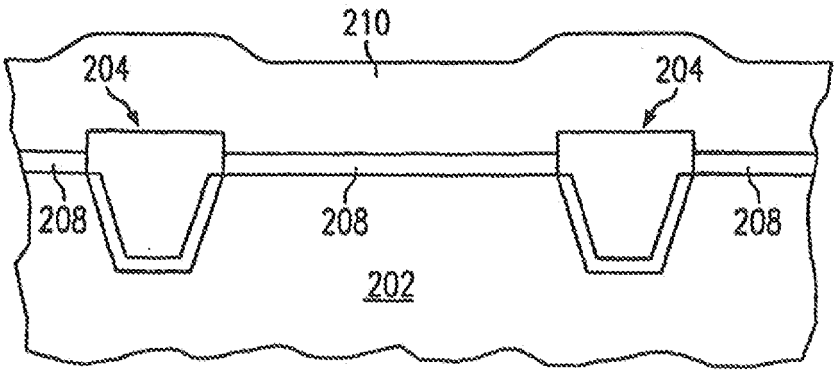

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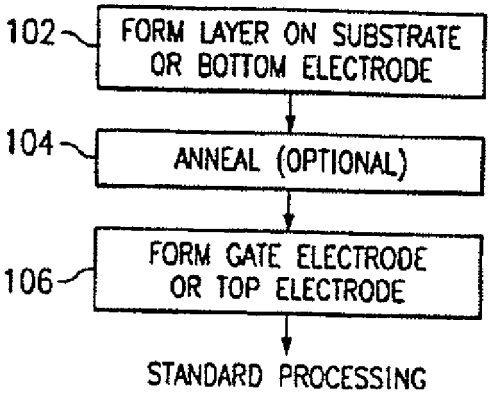
FIG. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 00 10 0195

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 4 464 701 A (ROBERTS STANLEY ET AL) 7 August 1984 (1984-08-07) * the whole document *	1-11	H01L21/316 C23C16/40 C23C16/42
Y	US 4 432 035 A (HSIEH NING ET AL) 14 February 1984 (1984-02-14) * claims 1-24 *	1-11	
Y	WO 98 59366 A (LAM RES CORP) 30 December 1998 (1998-12-30) * page 8 *	1-11	
X	DATABASE 'Online! retrieved from INSPEC Database accession no. 3058407 XP002150391 * abstract *	1-11	
P,X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 10, 31 August 1999 (1999-08-31) & JP 11 135774 A (TEXAS INSTR INC <TI>), 21 May 1999 (1999-05-21) * abstract *	1-11	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)
H01L
C23C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	18 October 2000	Wolff, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 10 0195

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